IDEC Chip Design Contest

# SvarogSoC
# A Low-Power Single Cycle RISC-V Microcontroller

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## 1. Introduction

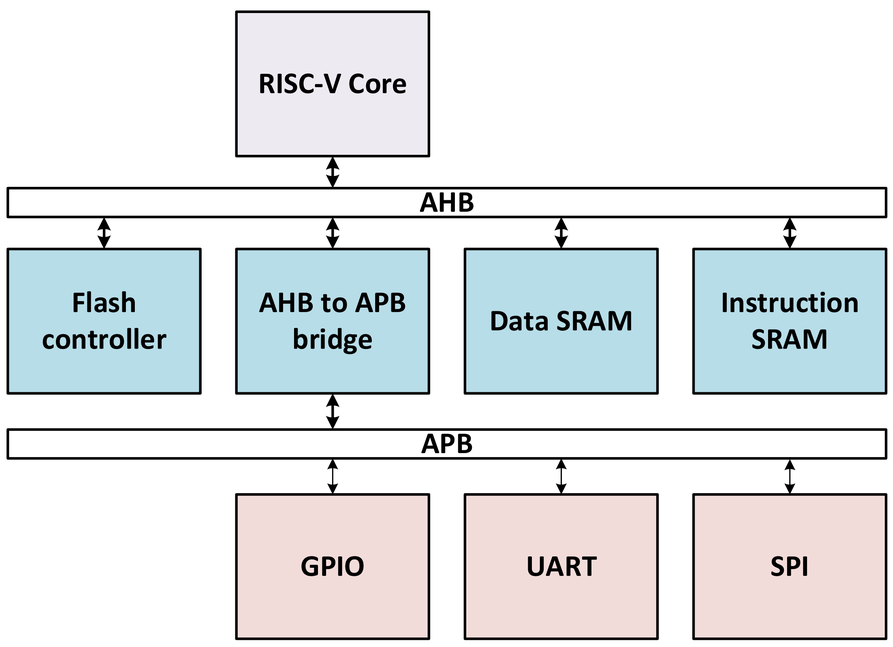
Self-powered devices impose strict constraints on power consumption of digital blocks. Design of low-power focused processor is crucial for long lifetime of autonomous systems. In this work, a simple processor called SvarogSoC is presented that can be used for controlling external circuitry and pre-processing of acquired data from sensors. The architecture, design flow and results are presented.

## 2. System design

### 2.1 SvarogSoC architecture

SvarogSoC consists of a RISC-V core with instruction cache, data and instruction SRAM, flash controller and a set of memory-mapped peripherals. The RISC-V ISA has been selected because it is open-source and easy to implement in its simplest form. The core is a single cycle processor compliant with RV32I ISA. The system is designed in SystemVerilog with maximum parametrization in mind. Memory blocks are connected to AMBA AHB interconnect with processor as bus master. In addition, peripherals are interfaced via AMBA APB.

### 2.2 System diagram

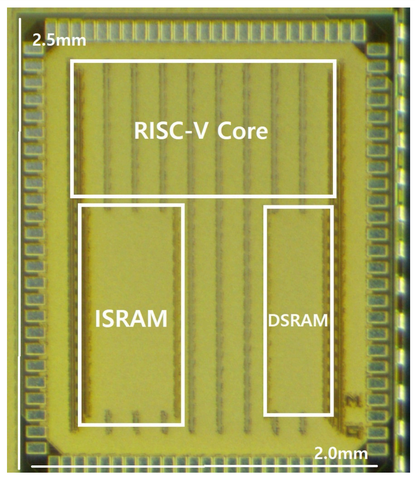



## 3. Chip implementation and testing

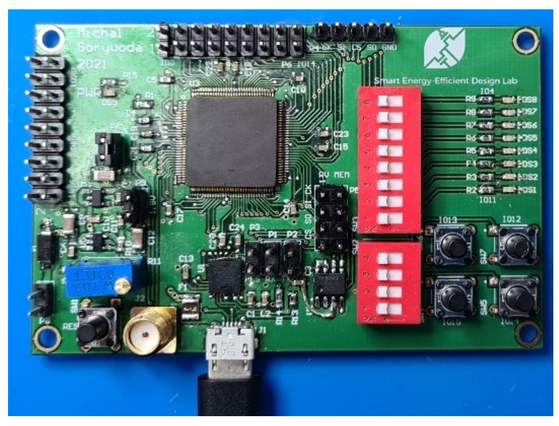
### 3.1 Design flow

Functional design was performed on RTL, synthesis and layout stages using Synopsys VCS + Verdi. RTL was synthesized using Synopsys Design Compiler
Mapped netlist was used as input to layout, performed in Synopsys ICC. Final sign-off and rule fixing was made in Cadence Virtuoso. Design used 100 pads and the die was bonded and sealed in QFN128 package.

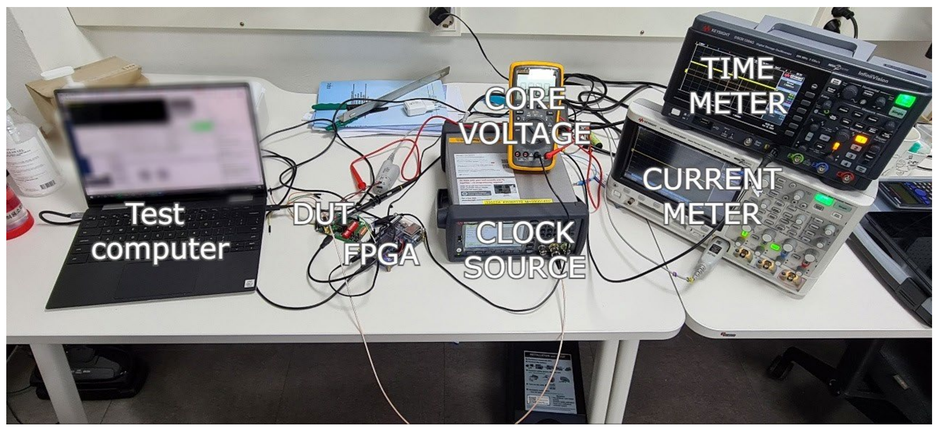
### 3.2 Die photography




### 3.3 PCB photography

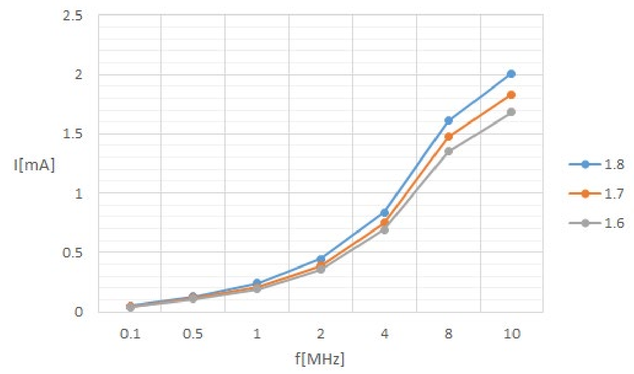



### 3.4 Test setup




### 3.5 Test results

A set of test benchmarks uploaded and their execution time measured. Core supply current measurement was performed for vvadd benchmark.




| Benchmark | $t_{exec}$[ms] |
|---|---|
| vvadd 200 | 9.28 |
| multiply 100 | 676 |
| mt-matmul 6x6 | 972 |
| mt-matmul 8x8 | 2278 |

TABLE I
BENCHMARK EXECUTION TIME @ 8MHZ, 1.8V

## 4. Conclusion

Benchmarks requiring multiplication operation are considerably slower than other programs. To solve this, future revisions will include RISC-V M extension for hardware multiplication support. The design can be used as a flexible supervisor block for digitally controlled analog and mixed-signal blocks.

## 5. Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

## 6. Reference

[1] “The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Document Version 2.2”, Editors Andrew Waterman and Krste Asanovic, RISC-V Foundation, May 2017. [Online] Available: https://riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf